Cirrus Logic, Inc.
Atty. Docket 0094-D1A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application Of:			
	Richard T. Behrens, et al	Group Art Unit:	Unassigned
Serial No:	Unassigned	Examiner:	Unassigned
Divisional of:	08/838,113		
Filed:	4/16/97		
Title:	Synchronous Read Channel		

PRELIMINARY AMENDMENT

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Please enter the following amendments before examination of the above identified patent application:

IN THE SPECIFICATION:

Please insert the following new paragraph at page 1, line 1 before "Background of the Invention":

This application is a divisional of copending application No. 08/838,113 filed 4/16/97, which is a divisional of U.S. Pat. No. 5,812,334 issued 9/22/98, which is a

continuation of U.S. Pat. 5,424,881, issued 6/13/95, both of which are hereby incorporated by reference in their entireties.

Please insert the following new paragraph at page 12, line 22:

Figure 7 is a state transition diagram for a sequence detector matched to a trellis code (RLL d=l constraint).

Please delete the paragraph beginning at line 3 on page 13.

Please replace the paragraph beginning at line 23 on page 14 with the following rewritten paragraph:

Figure 3 provides a block diagram illustrating the general organization of the CL-SH4400. As may be seen in Figure 3, the digitized read data for the CL-SH4400 is provided in an N-bit parallel form as digitized read data DRD0 and DRD1. Each of these two signals in the preferred embodiment disclosed is a 6-bit digitized read data signal. These two N-bit signals represent digitized samples of a read signal directly from a read head of the storage device after analog amplification and analog filtering. Those skilled in the art will recognize that the purpose of the analog amplifier and the analog filter is to scale the signals to the input range of the digital to analog converter and to attenuate frequencies above the Nyquist frequency (1/2 the sample frequency) to avoid signal distortion due to aliasing. In general, the analog filter will perform pulse shaping as well. The digitized read data signal DRD0 is a digitized read signal sample effectively taken near the center of a channel bit time (defined by the VFO frequency), subject however to a small amount of timing error or intentional timing set point offset in the VFO. The

digitized read data signal DRD1 is the corresponding digitized read sample effectively taken near the center time of the previous logical channel bit, subject of course to similar timing errors and timing set point offsets. These two digitized read data signals are processed in the CL- SH4400 in a parallel or simultaneous manner so that ultimately in the CL-SH4400, two successive bits of digital read data will be derived from one set of DRD0 and DRD1 signals which together with successive bit pairs are decoded by a run-length limited (RLL) decoder and derandomized if applicable (e.g. if initially randomized) to provide the NRZ data output stream of the device. The processing of two digitized read data samples simultaneously doubles the throughput of the CL-SH4400 for a given clock rate without doubling the circuitry required, particularly in the sequence detector, though the present invention is not specifically limited to processing of two digitized read data sample at a time. One could process one digitized read data sample at a time, or alternatively process more than two digitized read data samples at a time, if desired. In that regard, the number of N-bit digitized read data sample connections to the chip normally will equal the number of samples processed at a time, though such signals could be multiplexed so that the number of N-bit digitized read data samples connections to the chip is less than the number of samples processed together.

Please replace the paragraph beginning at line 26 on page 16 with the following rewritten paragraph:

In one mode of operation, multiplexer 28 couples the DRD0 and DRD1 signals directly to a transition detector 22 which processes the successive samples to detect the presence of transitions in each of the two digitized read data signals. In the preferred embodiment, the transition detector 22 is of the type disclosed in co-pending U.S. application for patent entitled Digital Pulse Detector, filed May 8, 1992 as Serial

No. 07/879,938, the disclosure of which co-pending application is incorporated herein by reference. The output of the transition detector is a low or high level during the respective bit times (delayed as described in the co-pending application) depending upon whether a transition (providing a high level output) or no transition (providing a low level output) was detected. The output of the transition detector 22, the peak detected signal PKDET, in this mode would be coupled to multiplexer 24 and through a sync mark detector 26 to provide a sync byte detected output SBD if a sync byte was in fact detected, and to couple the two bits to the RLL decoder 28 which decodes the bit stream to provide the NRZ data out digital data. In the preferred embodiment run length constraint violations are detected and optionally multiplexed onto the NRZ data out lines. These may be used by an error correcting system within the disk controller. In the preferred embodiment, an error tolerant sync mark detector 26 is used. This detector is designed to achieve a level of error tolerance for the synchronization function equal to that achieved for the data field by the error-correction code implemented in the disk controller. This is achieved in part by employing an error-tolerant Synchronization Mark pattern for minimum cross-correlation with the preamble and for minimum auto-correlation, and by making the number of four-channel-bit groups which must be detected programmable. The synchronization mark recovery procedure may be used to recover data when a severe defect has destroyed the entire synchronization mark. When using this mode, the CL-SH4400 first goes through a normal timing and gain acquisition procedure while counting channel bits. The synchronization mark is assumed to have been detected when the count matches the synchronization mark recovery count. By varying the synchronization mark recount, the microcontroller can vary the assumed starting point of a header or data area until the correct starting point is tried, whereupon the sector will be recovered if there is no other error beyond the capability of the error correction code in the disk controller.

Please replace the paragraph beginning at line 18 on page 18 with the following rewritten paragraph:

The output of the transition detector 22 in this mode is also provided to the gain control circuit 32 and the timing recovery circuit 34. Also the N-bit digitized samples DRDO and DRD1 are coupled through multiplexer 20 to the gain control circuit 22 and the timing recovery circuit 34. The gain control circuit 32 is shown in more detail in Figure 4. The gain errors (the difference between the programmable desired signal level referred to as the Gain Set point, and each digitized data signal) are determined for each digitized read data sample by the gain error circuit 33. The outputs PKDET of the transition detector 22 provide references to control the multiplexer 35 of the gain control circuit 32, as the gain adjustments are determined by the signal amplitudes of transitions and not the signal levels between transitions. The automatic gain control signal VGAC (5-bits in the preferred embodiment) for coupling back to the companion integrated circuit for analog amplifier gain control is provided by the digital gain loop filter 37. As shown therein, the gain loop filter includes a loop filter coefficient which is independently programmable for tracking and acquisition. The individual gain errors are also coupled to a channel quality circuit 46 as the signals GERR so that gain control performance can be measured to determine the best choice of loop filter coefficients and other parameters of the channel with respect to the performance of the automatic gain control loop.

Please replace the paragraph beginning at line 20 on page 19 with the following rewritten paragraph:

The timing recovery circuit 34 in the CL-SH4400 is shown in greater detail in Figure 5, and is generally in accordance with the timing recovery circuit disclosed in a

co-pending U.S. patent application entitled Timing Recovery Circuit For Synchronous Wave Form Sampling, filed September 30, 1992 as Serial No. 07/954,350, the disclosure of which is also incorporated herein by reference. Timing recovery and maintenance of synchronization, of course, can only be done upon the detection of a transition, as the absence of transitions contains no timing information. The timing recovery circuit controls the read clocks which are synchronized to the read wave form. In the timing recovery circuit, a phase detector 39 digitally computes the phase error in the sampling instants of the analog to digital converter on the companion chip from the digitized sample values during transitions, as indicated by the signals PKDET. Providing timing error corrections only at transition times reduces the noise (jitter) in the timing loop. The sequence of measured phase errors is digitally filtered by filter 41 to produce a frequency control signal which is fed back to the companion chip, in the preferred embodiment as the 5-bit frequency control signal FCTL.

Please replace the paragraph beginning at line 9 on page 21 with the following rewritten paragraph:

The timing recovery circuit 34 also includes a programmable timing set point. The timing set point permits a wider range of sampling strategies which enables the support of a wider range of pulse shapes. The timing set point is useful on retry in the event of the detection of an uncorrectable error. Also the digital filter includes two coefficients which are independently programmable for acquisition and tracking. These are also usable in a retry strategy to change the bandwidth and hence the response time of the timing loop. Like the individual gain errors GERR, the individual timing errors TERR are also coupled to the channel quality circuit for contribution to the quantitative analysis of the channel quality with respect to timing recovery. One alternate embodiment of the timing recovery block includes a frequency error detector. The

frequency error detector is used to decrease the time required for the timing loop to lock to the channel bit frequency and phase during the acquisition period before encountering data.

Please replace the paragraph beginning at line 4 on page 22 with the following rewritten paragraph:

As variations on the mode of operation just described, the two N-bit digitized read data signals DRD0 and DRD1 may be passed through a pulse shaping filter 38 prior to being coupled to multiplexing block 20. The pulse shaping filter provides digital filtering at the cost of a small amount of delay with two user selectable coefficients PC1 and PC2, independently programmable in the filter structure. This pulse shaping filter, of course, is in addition to any filtering done in the analog domain, and is an example of the flexibility and adaptability of the present invention. In particular, the effect of the pulse shaping filter may be eliminated by multiplexing block 20, or alternatively, the pulse shaping filter may be used with coefficients user selected, and thus variable, to provide the best performance of the overall storage system read channel with the flexibility to accommodate changes in pulse shape when changing from one recording zone to another, and to allow coefficient variations as part of overall device parameter variations for systematic retries upon the detection of uncorrectable errors in the subsequent error detection and correction (EDAC) operations. The pulse shaping filter of the preferred embodiment is a finite impulse response digital filter which means that the output is a function of the current and past inputs but not a function of its own past outputs. The delays necessary for the filter to remember the past inputs are shared by delay 36 to provide a separate delay path to multiplexing block 20. The delay path through delay 36 provides an amount of delay equivalent to the delay of pulse shaping filter 38. Multiplexing block 20 is provided to give a maximum of flexibility in modes of

usage, by providing a separate source of input for the transition detector and the group of blocks comprising the sequence detector 40 (by way of spectrum smoothing filter 42), the gain control circuitry 32 and the timing recovery circuitry 34. The multiplexing block is designed so that all blocks may operate upon the raw input samples provided by DRDO and DRD1, or alternatively the pulse shaping filter may be placed in one of the multiplexing block's output paths with the delay placed in the other path. The delay is necessary in this case so that the transition detector's outputs are synchronized with the sample values reaching the gain control circuitry and timing recovery circuitry. Finally, the pulse shaping filter may feed both of the multiplexing block's output paths. In general the multiplexing block could be designed so that by programming the multiplexing block each block at the multiplexing block's outputs (transition detector 22, gain control 32, timing recovery 34, and sequence detector 40 by way of spectrum smoothing filter 42) could receive raw input samples, delayed raw input samples, or filtered input samples independent of the data received by the other blocks. In the preferred embodiment of the present invention however, the gain control circuitry and the timing recovery circuitry have the capability of compensating for the pulse shape in an effort to increase the accuracy of the gain and timing recovery loops, and to reduce the amount of circuitry, the gain control circuitry and timing recovery circuitry assume the same pulse shape for which sequence detector 40 is programmed. This basic pulse shape received by the sequence detector is only marginally affected by the addition of the spectrum smoothing filter, which is designed to reduce only the head bumps at the tails of the pulse and does not seriously affect the center of the pulse except to correct for head bumps due to neighboring pulses. In that regard, the present invention includes a channel quality circuit 46 for measuring the quality of the read channel as earlier described. This provides not only quantitative channel evaluation, but in addition allows selection of read channel parameters such as, but not limited to, the coefficients PC1

and PC2 in the pulse shaping filter to best adapt the read channel to the characteristics of the storage medium and the pulse form and characteristics being read therefrom.

Please replace the paragraph beginning at line 1 on page 25 with the following rewritten paragraph:

The present invention further includes a sequence detector 40 which receives as its input the two N-bit digital read data signals DRD0 and DRD1 as may be modified by the pulse shaping filter 38 and as may be additionally modified by the spectrum smoothing filter 42. In that regard, the spectrum smoothing filter 42, as shown in Figure 6 hereof, contains two delays FD1 and FD2 and four coefficients SC1, SC2, SC3 and SC4, all of which are independently programmable. The delays may be programmed from 0 to 23 channel bit intervals. The entire spectrum smoothing filter, or just its precursor correcting portion 43, can be disabled. The spectrum smoothing filter is designed to reduce the undershoots from the finite pole tips of a thin film head, or to reduce the bumps from the secondary gap of a single or double-sided MIG head. In the frequency domain, the filter acts to smooth out undulations caused by head bumps. If the precursor is disabled, the delay of the filter is disabled, whereas if a head which is not subject to head bumps is used, the post-cursor may be disabled.

Please replace the paragraph beginning at line 3 on page 28 with the following rewritten paragraph:

If the present invention is realized in an embodiment wherein digitized read data is processed a single bit time's worth at a time, a Viterbi detector of a conventional design may be used, or if two or more bit time's worth of samples are to be processed simultaneously, as in the preferred embodiment of the present invention, a conventional Viterbi detector could be modified for that purpose. However, in the preferred

embodiment of the present invention, the uniquely modified form of Viterbi detector used is that disclosed in a co-pending application for patent entitled "Method and Apparatus for Reduced-Complexity Viterbi-type Sequence Detectors" filed March 16, 1992 as Serial No. 07/852,015, the disclosure of which is incorporated herein by reference.

Please replace the paragraph beginning at line 20 on page 30 with the following rewritten paragraph:

The sequence detector utilized in the CL-SH4400 can be programmed to operate on any channel response which can be well represented by sequences in the form of a, b, 1, c wherein the selection of a, b and c allow the ability to accommodate pulse asymmetry which might otherwise require that the read signal pass through an analog or digital phase equalizer prior to entering the sequence detector. The levels a, b and c also give the ability to select between center and side sampling. Center-sampled pulses are notably those for which the sample levels a, b, 1, and c are selected such that 1 is very near the peak of the pulse, b and c are roughly halfway down their respective sides of the pulse, and a is near zero, for example, the sample levels 0, 1/2, 1 and 1/2. Side-sampled pulses are notably those for which the sample levels are selected such that 1 and b (which is about 1) straddle the peak of the pulse, for example the sample levels 5/16, 1, 1 and 5/16. This choice of side versus center sampling also affects the manner in which gain error and phase error are calculated in the gain control loop and timing recovery loop. The option to choose between side and center sampling allows the user a wider range of possible trade-offs between the amount of equalization (filtering) used to shape the raw pulse shape into the target pulse shape of the sequence detector and the amount of noise enhancement which arises as a consequence of shaping the raw

pulse. Hence the read channel can be more suitably matched to the storage medium to provide better performance.

Please insert a new paragraph beginning at line 12 on page 31 as follows:

The state machine model for the partial response sequence detector **40** is shown in Figure 7. Note that the model embodies several kinds of information. First, the isolated pulse sample values a, b, 1, and c are included. Second, the alternating polarity of pulses constraint is enforced. Third, the minimum run-length constraint of d=l is enforced; that is, the state transition diagram is matched to a trellis code constraint.

Please delete the paragraph beginning at line 11 on page 34:

Please delete Appendices 1, 2, 3, 4 and 5.

IN THE CLAIMS:

Please cancel Claims 1-7.

Please add new claims 8-14:

8. An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal;

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby; and

an RLL(d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector.

9. The integrated circuit synchronous read channel of claim 8 further comprising digital pulse shaping filter circuitry for modification of the digitized read signals prior to

receipt thereof by at least one of (i) the sequence detector, (ii) digital peak detector and (iii) the timing recovery circuitry.

10. The integrated circuit synchronous read channel of claim 9 further comprising delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuitry to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter.

11. The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes variable filter parameters.

12. The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes programmable filter parameters.

13. The integrated circuit synchronous read channel of claim 9 further comprising spectrum smoothing filter circuitry for filtering the digitized read signals prior to processing by the sequence detector.

14. The integrated circuit synchronous read channel of claim 8 wherein the sequence detector processes two digitized read signals at a time, the two digitized read signals representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times.

IN THE DRAWINGS

Please add a new Figure 7 as attached hereto.

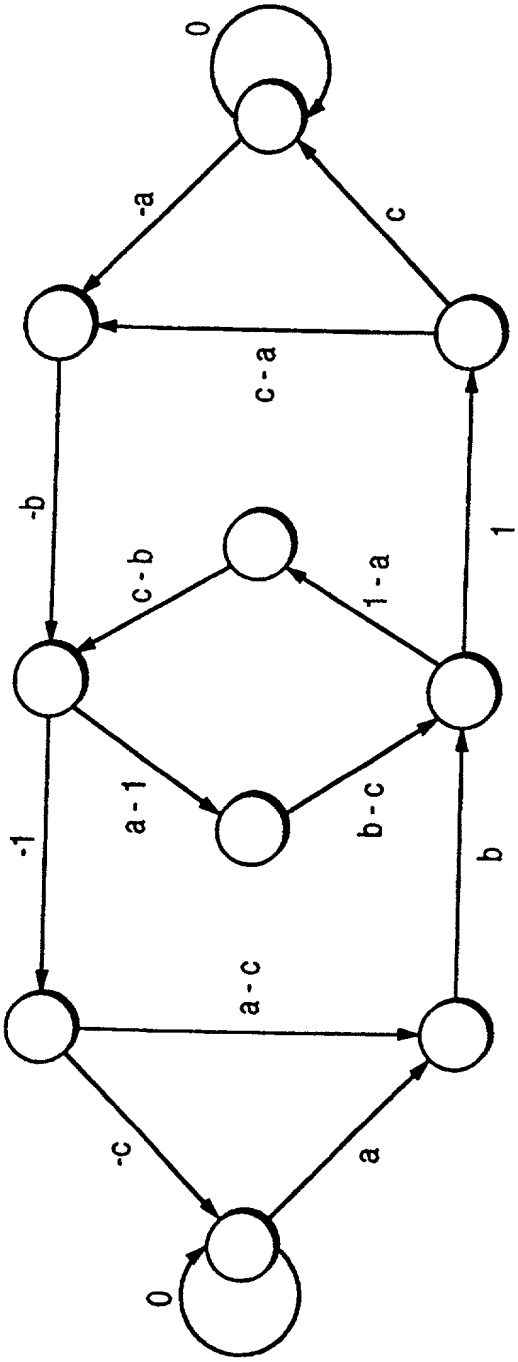

FIG. 7

CONCLUSION

The above amendments to the specification and claims do not add new matter, the Applicant has merely incorporated the relevant information from Appendices 1-5 into the main disclosure. The remainder of the Appendices has been deleted as unnecessary to the understanding and enablment of the present invention. Newly added Figure 7, showing the state machine model for the partial response sequence detector of the present invention, is disclosed in the original specification on page 27 of Appendix 1 as Figure 4.8-7. The Applicant respectfully requests the amendments be entered before examination of the present application.

Attached hereto is a marked-up version of the changes made by the current amendment, captioned **"Version with Markings to Show Changes Made"**.

Respectfully submitted,

Cirrus Logic, Inc.
4210 South Industrial Dr.
Austin, TX 78744
Customer No. 020284

Dan Shifrin
Reg. No. 34,473
303-464-6663

Date: Dec 21, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to The Assistant Commissioner for Patents, Washington , DC 20231, on:

12/21/01 (Date)

Dan Shifrin (Print Name)

(Signature)

#EI571068897US

Version with Markings to Show Changes Made

In the specification:

Insert the following new paragraph at page 1, line 1 before "Background of the Invention":

This application is a divisional of copending application No. 08/838,113 filed 4/16/97, which is a divisional of U.S. Pat. No. 5,812,334 issued 9/22/98, which is a continuation of U.S. Pat. 5,424,881, issued 6/13/95, both of which are hereby incorporated by reference in their entireties.

Insert the following new paragraph at page 12, line 22:

Figure 7 is a state transition diagram for a sequence detector matched to a trellis code (RLL d=l constraint).

The paragraph beginning at line 3 on page 13 has been deleted:

[There is attached hereto as Appendix 1 a preliminary data sheet entitled Sample Amplitude Digital R/W Channel, Part Number CL-SH4400 (hereinafter the CL-SH4400), the contents of which data sheet are incorporated herein by reference. This data sheet provides substantial information with respect to a preferred embodiment of the present invention as embodied in integrated circuits about to be introduced. Therefore, portions thereof will be referred to herein from time to time, either as providing support for the description to follow, or a specific example of the application of

the descriptions provided herein and in other co-pending applications also incorporated herein by reference.]

The paragraph beginning at line 23 on page 14 has been amended as follows:

Figure 3 provides a block diagram illustrating the general organization of the CL-SH4400. [This diagram is similar to the block diagram on page 1 of Appendix 1, though expanded somewhat to show additional details thereof.] As may be seen in Figure 3, the digitized read data for the CL-SH4400 is provided in an N-bit parallel form as digitized read data DRD0 and DRD1. Each of these two signals in the preferred embodiment disclosed is a 6-bit digitized read data signal. These two N-bit signals represent digitized samples of a read signal directly from a read head of the storage device after analog amplification and analog filtering. Those skilled in the art will recognize that the purpose of the analog amplifier and the analog filter is to scale the signals to the input range of the digital to analog converter and to attenuate frequencies above the Nyquist frequency (1/2 the sample frequency) to avoid signal distortion due to aliasing. In general, the analog filter will perform pulse shaping as well. The digitized read data signal DRD0 is a digitized read signal sample effectively taken near the center of a channel bit time (defined by the VFO frequency), subject however to a small amount of timing error or intentional timing set point offset in the VFO. The digitized read data signal DRD1 is the corresponding digitized read sample effectively taken near the center time of the previous logical channel bit, subject of course to similar timing errors and timing set point offsets. These two digitized read data signals are processed in the CL- SH4400 in a parallel or simultaneous manner so that ultimately in the CL-SH4400, two successive bits of digital read data will be derived from one set of DRD0 and DRD1 signals which together with successive bit pairs are decoded by a run-length limited (RLL) decoder and derandomized if applicable (e.g. if initially randomized) to

provide the NRZ data output stream of the device. The processing of two digitized read data samples simultaneously doubles the throughput of the CL-SH4400 for a given clock rate without doubling the circuitry required, particularly in the sequence detector, though the present invention is not specifically limited to processing of two digitized read data sample at a time. One could process one digitized read data sample at a time, or alternatively process more than two digitized read data samples at a time, if desired. In that regard, the number of N-bit digitized read data sample connections to the chip normally will equal the number of samples processed at a time, though such signals could be multiplexed so that the number of N-bit digitized read data samples connections to the chip is less than the number of samples processed together.

The paragraph beginning at line 26 on page 16 has been amended as follows:

In one mode of operation, multiplexer 28 couples the DRD0 and DRD1 signals directly to a transition detector 22 which processes the successive samples to detect the presence of transitions in each of the two digitized read data signals. In the preferred embodiment, the transition detector 22 is of the type disclosed in co-pending U.S. application for patent entitled Digital Pulse Detector, filed May 8, 1992 as Serial No. 07/879,938, the disclosure of which co-pending application is incorporated herein by reference. [The Background, Specification and Drawings from that application are attached hereto as Appendix 3.] The output of the transition detector is a low or high level during the respective bit times (delayed as described in the co-pending application) depending upon whether a transition (providing a high level output) or no transition (providing a low level output) was detected. The output of the transition detector 22, the peak detected signal PKDET, in this mode would be coupled to multiplexer 24 and through a sync mark detector 26 to provide a sync byte detected output SBD if a sync byte was in fact detected, and to couple the two bits to the RLL

decoder 28 which decodes the bit stream to provide the NRZ data out digital data. In the preferred embodiment run length constraint violations are detected and optionally multiplexed onto the NRZ data out lines. These may be used by an error correcting system within the disk controller. In the preferred embodiment, an error tolerant sync mark detector 26 is used. This detector [, described more fully in paragraph 4.9 on page 27 of Appendix 1,] is designed to achieve a level of error tolerance for the synchronization function equal to that achieved for the data field by the error-correction code implemented in the disk controller. This is achieved in part by employing an error-tolerant Synchronization Mark pattern for minimum cross-correlation with the preamble and for minimum auto-correlation, and by making the number of four-channel-bit groups which must be detected programmable. [As described in paragraph 4.9 on page 27 of Appendix 1, the] The synchronization mark recovery procedure may be used to recover data when a severe defect has destroyed the entire synchronization mark. When using this mode, the CL-SH4400 first goes through a normal timing and gain acquisition procedure while counting channel bits. The synchronization mark is assumed to have been detected when the count matches the synchronization mark recovery count. By varying the synchronization mark recount, the microcontroller can vary the assumed starting point of a header or data area until the correct starting point is tried, whereupon the sector will be recovered if there is no other error beyond the capability of the error correction code in the disk controller.

The paragraph beginning at line 18 on page 18 has been amended as follows:

The output of the transition detector 22 in this mode is also provided to the gain control circuit 32 and the timing recovery circuit 34. Also the N-bit digitized samples DRDO and DRD1 are coupled through multiplexer 20 to the gain control circuit 22 and the timing recovery circuit 34. The gain control circuit 32 is shown in more detail in

Figure 4. The gain errors (the difference between the programmable desired signal level referred to as the Gain Set point, and each digitized data signal) are determined for each digitized read data sample by the gain error circuit 33. The outputs PKDET of the transition detector 22 provide references to control the multiplexer 35 of the gain control circuit 32, as the gain adjustments are determined by the signal amplitudes of transitions and not the signal levels between transitions. The automatic gain control signal VGAC (5-bits in the preferred embodiment) for coupling back to the companion integrated circuit for analog amplifier gain control is provided by the digital gain loop filter 37 **[**, the details of which are shown in paragraph 4.5.2 on page 18 of Appendix 1**]**. As shown therein, the gain loop filter includes a loop filter coefficient which is independently programmable for tracking and acquisition. **[**The manner of actual calculation of the gain error in the CL-SH4400 is set forth in detail in paragraph 4.5.1 on page 17 of Appendix 1.**]** The individual gain errors are also coupled to a channel quality circuit 46 as the signals GERR so that gain control performance can be measured to determine the best choice of loop filter coefficients and other parameters of the channel with respect to the performance of the automatic gain control loop.

The paragraph beginning at line 20 on page 19 is amended as follows:

The timing recovery circuit 34 in the CL-SH4400 is shown in greater detail in Figure 5, and is generally in accordance with the timing recovery circuit disclosed in a co-pending U.S. patent application entitled Timing Recovery Circuit For Synchronous Wave Form Sampling, filed September 30, 1992 as Serial No. 07/954,350, the disclosure of which is also incorporated herein by reference. **[**The Background, Specification and Drawings from that application are attached hereto as Appendix 4.**]** Timing recovery and maintenance of synchronization, of course, can only be done upon the detection of a transition, as the absence of transitions contains no timing

information. The timing recovery circuit controls the read clocks which are synchronized to the read wave form. In the timing recovery circuit, a phase detector 39 digitally computes the phase error in the sampling instants of the analog to digital converter on the companion chip from the digitized sample values during transitions, as indicated by the signals PKDET. Providing timing error corrections only at transition times reduces the noise (jitter) in the timing loop. The sequence of measured phase errors is digitally filtered by filter 41 to produce a frequency control signal which is fed back to the companion chip, in the preferred embodiment as the 5-bit frequency control signal FCTL.

The paragraph beginning at line 9 on page 21 is amended as follows:

[In addition to the co-pending application just referred to, this is also described in paragraph 4.6.1 of page 19 of Appendix 1, with the digital filter for the compensation in the timing recovery loop being described in paragraph 4.6.2 thereof.] The timing recovery circuit 34 also includes a programmable timing set point. The timing set point permits a wider range of sampling strategies which enables the support of a wider range of pulse shapes. The timing set point is useful on retry in the event of the detection of an uncorrectable error. Also the digital filter includes two coefficients which are independently programmable for acquisition and tracking. These are also usable in a retry strategy to change the bandwidth and hence the response time of the timing loop. Like the individual gain errors GERR, the individual timing errors TERR are also coupled to the channel quality circuit for contribution to the quantitative analysis of the channel quality with respect to timing recovery. One alternate embodiment of the timing recovery block includes a frequency error detector. The frequency error detector is used to decrease the time required for the timing loop to lock to the channel bit frequency and phase during the acquisition period before encountering data.

The paragraph beginning at line 4 on page 22 is amended as follows:

As variations on the mode of operation just described, the two N-bit digitized read data signals DRD0 and DRD1 may be passed through a pulse shaping filter 38 prior to being coupled to multiplexing block 20. The pulse shaping filter provides digital filtering at the cost of a small amount of delay with two user selectable coefficients PC1 and PC2, independently programmable in the filter structure [of Figure 4.7-1 on page 21 of Appendix 1]. This pulse shaping filter, of course, is in addition to any filtering done in the analog domain, and is an example of the flexibility and adaptability of the present invention. In particular, the effect of the pulse shaping filter may be eliminated by multiplexing block 20, or alternatively, the pulse shaping filter may be used with coefficients user selected, and thus variable, to provide the best performance of the overall storage system read channel with the flexibility to accommodate changes in pulse shape when changing from one recording zone to another, and to allow coefficient variations as part of overall device parameter variations for systematic retries upon the detection of uncorrectable errors in the subsequent error detection and correction (EDAC) operations. The pulse shaping filter of the preferred embodiment is a finite impulse response digital filter which means that the output is a function of the current and past inputs but not a function of its own past outputs. The delays necessary for the filter to remember the past inputs are shared by delay 36 to provide a separate delay path to multiplexing block 20. The delay path through delay 36 provides an amount of delay equivalent to the delay of pulse shaping filter 38 [(Figure 3 hereof differs from the functional block diagram on page 1 of Appendix 1 in that the delay circuit 36 is shown to also connect to the pulse shaping filter to illustrate the sharing of memory elements between the delay and the pulse shaping filter in the preferred embodiment.)] Multiplexing block 20 is provided to give a maximum of flexibility in modes of usage, by providing a separate source of input for the transition detector and the group of blocks

comprising the sequence detector 40 (by way of spectrum smoothing filter 42), the gain control circuitry 32 and the timing recovery circuitry 34. The multiplexing block is designed so that all blocks may operate upon the raw input samples provided by DRDO and DRD1, or alternatively the pulse shaping filter may be placed in one of the multiplexing block's output paths with the delay placed in the other path. The delay is necessary in this case so that the transition detector's outputs are synchronized with the sample values reaching the gain control circuitry and timing recovery circuitry. Finally, the pulse shaping filter may feed both of the multiplexing block's output paths. In general the multiplexing block could be designed so that by programming the multiplexing block each block at the multiplexing block's outputs (transition detector 22, gain control 32, timing recovery 34, and sequence detector 40 by way of spectrum smoothing filter 42) could receive raw input samples, delayed raw input samples, or filtered input samples independent of the data received by the other blocks. In the preferred embodiment of the present invention however, the gain control circuitry and the timing recovery circuitry have the capability of compensating for the pulse shape in an effort to increase the accuracy of the gain and timing recovery loops, and to reduce the amount of circuitry, the gain control circuitry and timing recovery circuitry assume the same pulse shape for which sequence detector 40 is programmed. This basic pulse shape received by the sequence detector is only marginally affected by the addition of the spectrum smoothing filter, which is designed to reduce only the head bumps at the tails of the pulse and does not seriously affect the center of the pulse except to correct for head bumps due to neighboring pulses. In that regard, the present invention includes a channel quality circuit 46 for measuring the quality of the read channel as earlier described. This provides not only quantitative channel evaluation, but in addition allows selection of read channel parameters such as, but not limited to, the coefficients PC1 and PC2 in the pulse shaping filter to best adapt the read channel to the characteristics of the storage medium and the pulse form and characteristics being read therefrom.

The paragraph beginning at line 1 on page 25 is amended as follows:

The present invention further includes a sequence detector 40 which receives as its input the two N-bit digital read data signals DRD0 and DRD1 as may be modified by the pulse shaping filter 38 and as may be additionally modified by the spectrum smoothing filter 42. In that regard, the spectrum smoothing filter 42, as shown in Figure 6 hereof [and Figure 4.7-3 on page 22 of Appendix 1], contains two delays FD1 and FD2 and four coefficients SC1, SC2, SC3 and SC4, all of which are independently programmable. The delays may be programmed from 0 to 23 channel bit intervals. The entire spectrum smoothing filter, or just its precursor correcting portion 43 [(SC1, SC2 and SD1 in Figure 4.7-3 of Appendix 1)], can be disabled. The spectrum smoothing filter is designed to reduce the undershoots from the finite pole tips of a thin film head, or to reduce the bumps from the secondary gap of a single or double-sided MIG head. In the frequency domain, the filter acts to smooth out undulations caused by head bumps. If the precursor is disabled, the delay of the filter is disabled, whereas if a head which is not subject to head bumps is used, the post-cursor may be disabled.

The paragraph beginning at line 3 on page 28 is amended as follows:

If the present invention is realized in an embodiment wherein digitized read data is processed a single bit time's worth at a time, a Viterbi detector of a conventional design may be used, or if two or more bit time's worth of samples are to be processed simultaneously, as in the preferred embodiment of the present invention, a conventional Viterbi detector could be modified for that purpose. However, in the preferred embodiment of the present invention, the uniquely modified form of Viterbi detector used is that disclosed in a co-pending application for patent entitled "Method and Apparatus for Reduced-Complexity Viterbi-type Sequence Detectors" filed March 16,

1992 as Serial No. 07/852,015, the disclosure of which is incorporated herein by reference. [The Background, Specification and Drawings from that application are attached hereto as Appendix 5.]

The paragraph beginning at line 20 on page 30 is amended as follows:

[As noted on page 26 of Appendix 1, the] The sequence detector utilized in the CL-SH4400 can be programmed to operate on any channel response which can be well represented by sequences in the form of a, b, 1, c wherein the selection of a, b and c allow the ability to accommodate pulse asymmetry which might otherwise require that the read signal pass through an analog or digital phase equalizer prior to entering the sequence detector. The levels a, b and c also give the ability to select between center and side sampling. Center-sampled pulses are notably those for which the sample levels a, b, 1, and c are selected such that 1 is very near the peak of the pulse, b and c are roughly halfway down their respective sides of the pulse, and a is near zero, for example, the sample levels 0, 1/2, 1 and 1/2. Side-sampled pulses are notably those for which the sample levels are selected such that 1 and b (which is about 1) straddle the peak of the pulse, for example the sample levels 5/16, 1, 1 and 5/16. This choice of side versus center sampling also affects the manner in which gain error and phase error are calculated in the gain control loop and timing recovery loop [(the details of this appear in Appendix 1)]. The option to choose between side and center sampling allows the user a wider range of possible trade-offs between the amount of equalization (filtering) used to shape the raw pulse shape into the target pulse shape of the sequence detector and the amount of noise enhancement which arises as a consequence of shaping the raw pulse. Hence the read channel can be more suitably matched to the storage medium to provide better performance.

Insert a new paragraph beginning at line 12 on page 31 as follows:

The state machine model for the partial response sequence detector **40** is shown in Figure 7. Note that the model embodies several kinds of information. First, the isolated pulse sample values a, b, 1, and c are included. Second, the alternating polarity of pulses constraint is enforced. Third, the minimum run-length constraint of d=l is enforced; that is, the state transition diagram is matched to a trellis code constraint.

The paragraph beginning at line 11 on page 34 is deleted:

[Also attached hereto as Appendix 2 is a preliminary data sheet for another embodiment of the present invention, namely part number CL-SH3300, which data sheet is also incorporated herein by reference. This integrated circuit incorporates the essential functions of the CL-SH4400 and the companion integrated circuit in a single integrated circuit.]

Appendices 1, 2, 3, 4 and 5 are deleted.

In the claims:

Claims 1-7 have been cancelled.

New claims 8-14 have been added:

8. (new) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal;

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby; and

an RLL(d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector.

9. (new) The integrated circuit synchronous read channel of claim 8 further comprising digital pulse shaping filter circuitry for modification of the digitized read

signals prior to receipt thereof by at least one of (i) the sequence detector, (ii) digital peak detector and (iii) the timing recovery circuitry.

10. (new) The integrated circuit synchronous read channel of claim 9 further comprising delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuitry to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter.

11. (new) The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes variable filter parameters.

12. (new) The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes programmable filter parameters.

13. (new) The integrated circuit synchronous read channel of claim 9 further comprising spectrum smoothing filter circuitry for filtering the digitized read signals prior to processing by the sequence detector.

14. (new) The integrated circuit synchronous read channel of claim 8 wherein the sequence detector processes two digitized read signals at a time, the two digitized read signals representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times

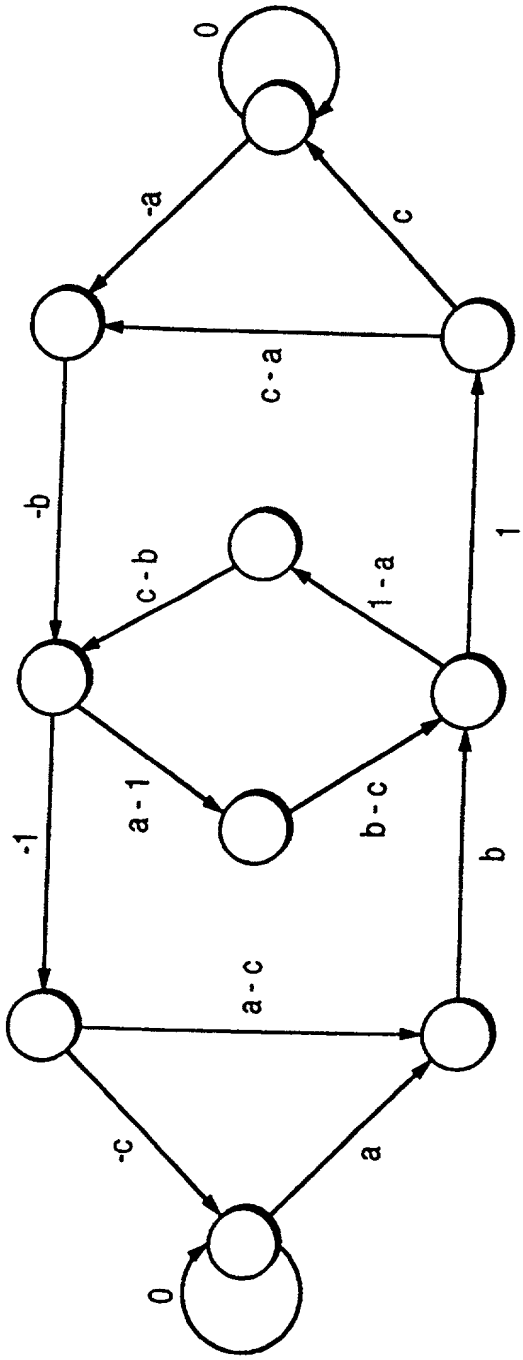

FIG. 7